

("Ugon"). Claim 1 has been canceled, rendering this rejection moot with regard thereto. However, Applicants respectfully traverse this rejection with regard to claims 5-7.

As discussed in the specification, the microprocessors contained within smart cards have current consumptions which depend on the calculations made inside the card. Thus a cryptographic calculation comprising a calculation tree which depends on the digits of the key used will have different current consumption footprints according to the value of the key used. As a result a fraudster could correlate the current consumption footprint of the key used and thus go back to the value of the key.

Accordingly, independent claim 5, as amended, defines a device for hiding operations performed by a component of a smart card, the smart card comprising an EEPROM memory and a microprocessor. The device includes, inter alia, means for modifying the current consumption of the component during the performance of said operations, wherein the means is configured to initiate a write or erase operation in a portion of the EEPROM memory simultaneous with an operation of the microprocessor in the smart card.

Ugon discloses a method of ensuring that a data carrier (i.e., a card) consumes the same amount of current whether the request operation is authorized or unauthorized. This is achieved by storing a bit in memory in either event (i.e., authorized or unauthorized) as opposed to only storing a bit when an operation is authorized (see the abstract and column 8, lines 11-53 of Ugon).

It is well known that in order to support a rejection under 35 U.S.C. §102, the applied reference must teach each and every claimed element. In the present case, independent claim 5 is not anticipated by Ugon for at least the reason that Ugon fails to disclose a device for hiding operations performed by a component of a smart card as claimed.

The Office Action asserts that Ugon discloses all of the elements of claim 5 inasmuch as Ugon discloses means for modifying electrical current consumption of a component during the performance of operations. To support this assertion, the Office

Action points to the abstract and column 8, lines 24-53 of Ugon. This assertion is unfounded for the following reasons.

The cited passage (i.e., column 8, lines 24-53) discloses that writing an access bit or an error bit into the memory in one or other of the two eventualities (key correct or key incorrect) always results in the data carrier consuming the same amount of electrical current, therefore a would-be defrauder attempting to monitor the strength of current to the card will always see a constant consumption whether the key used is correct or incorrect. However, nowhere in the passage or elsewhere in Ugon, is there any disclosure of the modifying means being configured to initiate a write or erase operation in a portion of the EEPROM memory simultaneous with an operation of the microprocessor in said smart card. Accordingly, claim 5 is not anticipated by Ugon.

Claims 6 and 7 depend from independent claim 5. Therefore, claims 6 and 7 are patentably distinguishable over Ugon for at least those reason presented above with respect to claim 5. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1 and 5-7 under 35 U.S.C. §102(b) in view of Ugon.

In the event that this rejection is maintained in a future action, Applicants respectfully request that the Examiner point out by column and line number where each element of the rejected claim is disclosed by Ugon in order to provide Applicants with sufficient information with which to respond.

In the third paragraph of page 2, the Office Action rejects claims 1, 3, 4 and 7 under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 4,932,053 to Fruhauf et al. ("Fruhauf"). Claims 1, 3 and 4 have been canceled, rendering this rejection moot with regard thereto. However, Applicants respectfully traverse this rejection with regard to claim 7.

Fruhauf discloses a protection circuit for protecting against unauthorized detection of protected data contained in "chip cards." The protection circuit comprises several simulation cells controlled by a pseudo-random sequence generator so that each cell is pseudo-randomly in one state or another. However, nowhere in Fruhauf is there any disclosure of a device for hiding current consumption that includes modifying means

configured to initiate a write or erase operation in a portion of the EEPROM memory simultaneous with an operation of the microprocessor in said smart card. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 3, 4 and 7 under 35 U.S.C. §102(b) in view of Fruhauf.

In the fourth paragraph of page 2, the Office Action rejects claims 1, 5 and 7 under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,813,024 to Lisimaque et al. ("Lisimaque"). Claim 1 has been canceled, rendering this rejection moot with regard thereto. However, Applicants respectfully traverse this rejection with regard to claims 5 and 7.

Lisimaque discloses an integrated circuit for confidential storage and processing of data. The circuit includes, among other things, a simulation cell which is activated when a comparator indicates that an access key is confirmed (i.e., the right key) to draw an electrical current identical to the current drawn by the writing of an error bit in memory when the access key is wrong. However, nowhere in Lisimaque is there any disclosure of a modifying means that is configured to initiate a write or erase operation in a portion of the EEPROM memory simultaneous with an operation of the microprocessor in said smart card. Therefore, claims 5 and 7 are not anticipated by Lisimaque. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 5 and 7 under 35 U.S.C. §102(b) in view of Lisimaque.

In the second paragraph of page 3, the Office Action rejects claim 2 under 35 U.S.C. §103 as allegedly being unpatentable over Ugon. Applicants respectfully traverse this rejection.

It is well known that in order to support a rejection under 35 U.S.C. §103, three basic criteria must be met. A first of the three criteria is that there must be some motivation or suggestion to modify the applied reference(s). As stated in §2143.01 of the MPEP, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination."

The Office Action asserts that it would have been obvious to modify the teaching of Ugon to include a voltage regulator in order to regulate the voltage supplied to the device. However, nowhere in Ugon is there any disclosure or suggestion of the desirability of regulating the voltage supplied to the device. Accordingly, absent proper motivation to modify the teachings of Ugon, the rejection of claim 2 under 35 U.S.C. §013 is improper.

Another of the three criteria is that the modification must teach each and every claimed element. In the present case, claim 2 is not rendered unpatentable over the modified teachings of Ugon for at least the reason that the modification fails to disclose or suggest each and every claimed feature.

Claim 2 defines a device for hiding operations performed by a component of a smart card. The device includes, inter alia, a modifying means that comprises at least one circuit for integrating the current of the component so as to average the variations in the current over time. As discussed above, Ugon discloses a method of ensuring that a card consumes the same amount of current whether a requested operation is authorized or not. However, nowhere in Ugon is there any disclosure of a circuit for integrating the current of the component so as to average the variations in the current over time.

The Office Action takes Official Notice that "using a capacitor or voltage regulator to integrate current consumption" is old and well known in the art. Applicants respectfully traverse this assertion.

As stated in the 3<sup>rd</sup> Edition of the Electronics Engineer's Handbook, "[t]he function of a voltage regulator is to maintain a constant output-voltage, *irrespective* of the changes of the input voltage or the *output current*" (emphasis added)<sup>1</sup>. Accordingly, Applicants assert that it is not known to use a voltage regulator to "integrate current" nor is such a result inherent from its use. Accordingly, should the Examiner maintain this rejection in a future action, Applicants respectfully request that the Examiner provide evidence of the common use of voltage regulators to "integrate current consumption."

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<sup>1</sup>Fink et al. editors, Electronic Engineer's Handbook, McGraw Hill, New York, 1989 p. 8-60.

Since Ugon fails to disclose a circuit for integrating the current of the component as claimed, and the use of a voltage regulator to regulate voltage does not inherently integrate current, the modification of Ugon to include a voltage regulator cannot possibly disclose a circuit as claimed. Therefore, even if one skilled in the art were motivated to modify the teachings of Ugon to include a voltage regulator as suggested by the Office Action, the modification would still fail to render claim 2 unpatentable for at least the reason that the modified teaching fails to disclose each and every claimed element.

Furthermore, even if the use of a voltage regulator did regulate current as asserted by the Office Action, there is no need to modify the current in Ugon. The system of Ugon consumes the same amount of current whether the request operation is authorized or not, therefore, there is no need to integrate the current according to Ugon. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 2 under 35 U.S.C. §103.

The application is in condition for allowance. Notice of same is earnestly solicited. Should the Examiner have any questions regarding this application, the Examiner is invited to call the undersigned at the telephone number provided below.

Respectfully submitted,

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ATTACHMENT

2. (Amended) A device [according to Claim 1] for hiding operations performed by a component intended to be integrated into a smart card, the device comprising:

means for modifying electrical current consumption of said component during performance of said operations, [wherein] said means for modifying [the current consumption comprises] comprising at least one circuit for integrating the current of the component so as to average the variations in this current over time.

5. (Amended) A device [according to Claim 1] for hiding operations performed by a component of a smart card, the smart card comprising an EEPROM memory and a microprocessor, the device comprising:

means for modifying electrical current consumption of said component during the performance of said operations, wherein said means for modifying the current consumption of the component [performs an operation of writing to or erasing] is configured to initiate a write or erase operation in a portion of the EEPROM memory simultaneous with an operation of [a] the microprocessor in said smart card.

6. (Amended) A device according to Claim 5, wherein [a] the portion of said memory is dedicated to the recording of a random data item.

7. (Amended) A device according to claim [1] 5, wherein the activation of the means of modifying the current consumption is controlled by a microprocessor so as to be activated solely for the operations to be protected.